Pap2858 #2 BT 4-19-02

TSMC-01-231

March 18, 2002

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
20 McIntosh Drive
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/043,864 01/10/02

K.T. Chen et al.

A METHOD AND APPARATUS TO ESTIMATE BURN-IN TIME BY MEASUREMENT OF SCRIBE-LINE DEVICES, WITH STACKING DEVICES, AND WITH COMMON PADS

Grp. Art Unit: 2858

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on March 22, 2002.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 3/22/02

U.S. Patent 5,981,971 to Miyakawa, "Semiconductor ROM Wafer Test Structure, and IC Card," describes a semiconductor ROM wafer test structure, and IC card.

Analysis and Design of Digital Integrated Circuits, second Edition, David A. Hodges & Horace G. Jackson, McGraw-Hill, New York, Chinese Edition, c. 1983, pp. 371-375, discusses MOS decoders.

U.S. Patent 6,157,046 to Corbett et al., "Semiconductor Reliability Test Chip," describes a semiconductor test chip.

U.S. Patent 5,835,552 to Kusumoto et al., "Time Counting Circuit and Counter Circuit," discloses a time counting circuit and counter circuit.

U.S. Patent 5,818,895 to Oh, "High-Speed Counter Circuit," discloses a high speed counter circuit.

U.S. Patent 5,619,437 to Nagai, "Parallel Data Counter Circuit," discloses a Parallel data counter circuit.

U.S. Patent 6,233,184 to Barth et al., "Structures for Wafer Level Test and Burn In," describes sturctures for wafer level test and burn-in.

U.S. Patent 6,064,213 to Khandros et al., "Wafer-Level Burn-In and Test," describes a wafer-level burn-in and test system that allows a wafer containing integrated circuits to be stressed and evaluated to conduct burn-in of the wafer to assure correct functioning of the wafer.

U.S. Patent 6,246,075 to Su et al., "Test Structures for Monitoring Gate Oxide Defect Densities and the Plasma Antenna Effect," describes an ensemble of test structures for monitoring gate oxide defect densities and plasma antenna effects.

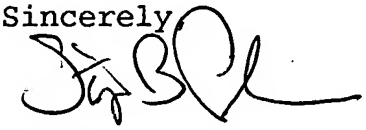
The following two U.S. Patents describe methods where a wafer containing memory devices, such as a DRAM (dynamic random access memory) are subjected to a burn-in operation of the memory device:

1) U.S. Patent 5,946,248 to Chien et al., "Method for Burn-In Operation on a Wafer of Memory Devices."
2) U.S. Patent 5,995,428 to Chien et al., "Circuit for Burn-In Operation on a Wafer of Memory Devices."

U.S. Patent 5,057,441 to Gutt et al., "Method for Reliability Testing Integrated Circuit Metal Films," describes a method for reliability testing integrated circuit metal films using a noise measurement technique.

U.S. Patent 5,808,947 to McClure, "Integrated Circuit that Supports and Method for Wafer-Level Testing," teaches an integrated circuit that includes both a wafer test-mode path that is operable to carry a wafer test-mode signal and a wafer power-supply path that is operable to carry a wafer power-supply signal.

Sincerely,



Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
T8mc-01-231	10/043,864
Applicant K.T. Chen et al.	
Filing Date 01/10/02	**Group Art Unit** 2858

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	5981971	11/9/99	Miyakawa	257	48	3/13/98
	6157046	12/500	Corbett et al.	257	48	4/23/99
	5835552	11/10/98	Kusumoto et al	377	24	11/12/96
	5818895	10/6/98	Oh	337	118	5/15/96
	5619437	4/8/97	Nagai	364	715.09	9/27/95
	6064213	5/16/00	Khandros et al.	324	754	1/15/97
	6246075	6/12/01	Su et al.	257	48	2/22/00
	5946248	8/31/99	Chien et al.	365	201	2/27/98
	5995428	11/30/99	Chien et al.	365	201	2/27/98
	5057441	10/15/91	Gutt et al.	437	8	10/29/90
	5808947	9/15/98	McClure	365	201	9/17/96

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Hodges et al., "Analysis and Design of Digital Integrated Circuits", second edition, David A. Hodges & Horace G. Jackson, Mc Graw-Hill, New York, Chinese Edition, c. 1983, pp. 371-375.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

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01/10/02	2858

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6233184	5/15/01	Barth et al.	365	201	11/13/98

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	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

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